Revolutionary Memories from Carbon Nanotube Technology

Supporting/Contributing Agencies: National Reconnaissance Office

A critical need exists to provide a universal memory technology that can simultaneously meet the needs of national security space and terrestrial systems. This universal memory technology will include low density to very high density applications, over a wide range of operating speeds, and meet stringent power, reliability and radiation performance requirements. At present no one technology can meet this need. However, carbon nanotube (CNT) nanotechnology has the potential to satisfy this diverse set of requirements. Specifically, CNT technology can provide a sufficiently flexible approach to provide:

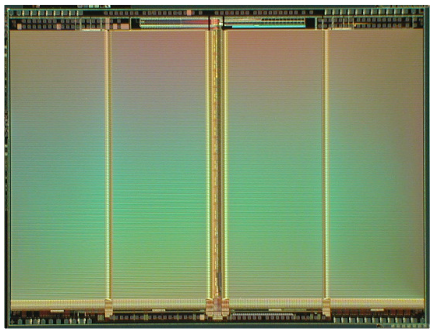
- High speed operation (nsec)
- Very high density (Gigabits) based on a very small memory cell area requirement (~ $6F^2$)
- Low power (virtually zero static leakage current and low dynamic power).
- Capable of either volatile or non-volatile operation as a function of design

STS-125 NRAM™

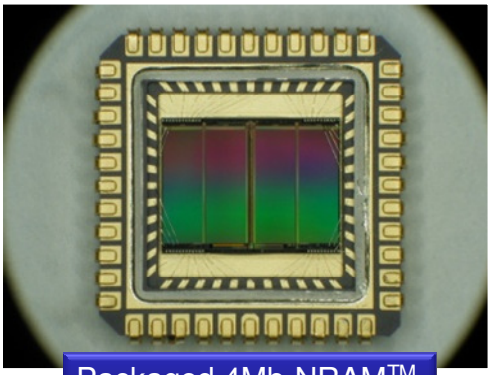
The efficacy of CNT memory technology has been demonstrated as a 16kbit Static Random Access (SRAM) device, fabricated at ON Semiconductor and the National Semiconductor Corporation, using technology originally developed by Nantero, and flown as an experiment on the May 2008 Hubble Repair Mission (STS-125). Fig 1 show the NRAM™ board flown on STS-125 (**Press release: http://www.lockheedmartin.com/news/press_releases/2009/1118_ss_nanotubes.html**)

In May 2008, this same technology was transferred to BAE Systems for integration into a radiation hardened manufacturing process. Lockheed Martin (which purchased Nantero) and BAE are jointly developing a radiation hardened 4Mbit CNT-based Non-Volatile, Nanotube Random Access Memory (NRAM) using a hardened 150nm process. Initial R&D has shown that, based on the lower power and area needs to support a CNT-based non-volatile memory cell, storage devices >2Gbit using a 90nm host technology are possible. In addition, as a complement to the above noted programs, efforts are underway to develop an embedded CNT memory technology that can support Application Specific Integrated Circuit (ASIC), microprocessor cache memory and Field Programmable Gate Array (FPGA) configuration control and block memory applications.

Figure 2 below shows a magnified image of a CNT memory array and a delidded packaged NRAM™ device, wire-bonded into the package.



Optical image of 4Mb array



Packaged 4Mb NRAM™